OBIRCH Dual Power Circuit

[0001] This application claims the benefit of U.S. Provisional Application No. 60/509,101, filed on October 6, 2003, entitled OBIRCH Dual Power Circuit, which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates generally to the testing of integrated circuits using the OBIRCH (Optical Beam Induced Resistance Change) techniques, and more particularly to the use of using the OBIRCH power supply to also power the integrated core circuits under test.

BACKGROUND

[0003] As is well known by those skilled in the art, a continuing goal in manufacturing and production of semiconductors is a reduction in size of components and circuits with the concurrent result of an increase in the number of circuits and/or circuit elements such as transistors, capacitors, etc., on a single semiconductor device. This relentless and successful reduction in size of the circuit elements has also required reduction in the size of the conductive lines, connecting devices and circuits. However, as the individual circuits and conducting lines are designed to be smaller and smaller, the number of circuits and connecting lines is increasing. This increase in numbers simultaneously raises the opportunity for more open circuits, more short circuits and other failures. The smaller size also increases the difficulty of identifying problem areas and/or failures such as short circuits and open circuits. As will be appreciated by those skilled in the art, these difficulties have led to the development of the OBIRCH testing techniques such as for example, described in Proceedings of the ATS (Asian Testing Symposium) 1997/11/17, AKITA, pp. 214-219 (1997).

[0004] Aluminum is one of the materials commonly used as the metal interconnect lines and silicon oxide is commonly used as the dielectric. Deterioration of the reliability of aluminum interconnection lines has become more serious with the progressive miniaturization of semiconductor integrated circuits and increase in interconnection levels of semiconductor integrated circuits. Deterioration of the reliability of aluminum interconnection lines is attributable to increase in current stresses and mechanical stresses induced in aluminum interconnection lines.

[0005] While the size of aluminum interconnection lines is on the submicron order, currents that flow through aluminum interconnection lines are on the order of several hundred microamperes and current density is as high as the order of 105 A/cm2. Further, mechanical stresses are induced in interconnection lines when the semiconductor integrated circuit is subjected to heat treatment in the LSI manufacturing process.

[0006] Such stresses induced in the interconnection lines cause the migration of aluminum atoms, electromigration or stress migration, which forms voids in the interconnection lines. These voids increase the resistance of the interconnection lines and, in the worst case, break the interconnection lines.

[0007] However, newer manufacturing techniques now favor copper as the metal for interconnect lines and various low K materials (organic and inorganic) are favored as the dielectric material. Aluminum interconnects may be formed by depositing a layer of aluminum and then using photoresist, lithography, and etching to leave a desired pattern of aluminum lines, the formation of copper interconnect lines are typically formed by a process now commonly referred to as a Damascene process. The Damascene process is almost the reverse of etching,

and simply stated a trench, canal or via is cut, etched or otherwise formed in the underlying dielectric and is then filled with metal (i.e., copper).

[0008] Unfortunately, although copper has the advantages discussed above, it readily diffuses into dielectric material used in the manufacture of semiconductor devices, and it diffuses especially easily into silicon dioxide. Diffusion of copper into the dielectric materials of a semiconductor device can cause serious reliability problems including electrical shorts. Therefore, it is typical to form a barrier layer between the copper used for conductors and leads and the dielectric material of a semiconductor device. Typical barrier layers may be formed of Ta (tantalum), TaN (tantalum nitride), Ti (titanium), TiN (titanium nitride) and various combinations of these metals as well as other metal. The barrier layer is typically formed on the bottom and sidewalls of the trenches and vias of the copper interconnects to prevent the copper from diffusing into the surrounding silicon dioxide as other dielectric material. A layer of silicon nitride is then typically deposited as a cover layer over the complete structure including the conductor areas and the dielectric layer before another layer or level of dielectric structure is deposited.

[0009] Accordingly, whether the integrated circuits (IC's) are fabricated using copper or aluminum interconnecting lines, the detection and observation of the frequency and positions of voids or shorts in the interconnecting lines, whether copper or aluminum, are essential to the reliability of integrated circuits.

[0010] Furthermore, as the size of the integrated circuits continues to decrease, the voltage levels for operating the individual elements has also decreased. Consequently, background noise and instability or drift of the power supplies used to test the circuits has a growing adverse effect on the ability to successfully test the IC's and to identify and locate the problems.

[0011] Therefore it would be advantageous to reduce the effects of background noise and power supply drift caused by the power supplies used during testing.

SUMMARY OF THE INVENTION

[0012] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by the present invention, which discloses methods and apparatus for reducing noise and power supply instability problems during OBIRCH analysis testing of circuit elements requiring a precise operating or core voltage. The invention comprising the steps of providing an OBIRCH analysis circuit having I/O terminals and having a circuit element to be tested connected thereto. A power source having a positive and a negative output is connected across the I/O terminals for providing a precise voltage to the OBIRCH analysis circuit. A diode circuit is also connected across the positive and negative outputs of the power source and includes a common or bi-polar diode having its anode connected to the positive output and its cathode connected to the anode of a plurality of Schottky diodes serially connected, cathode-to-anode. The negative output of the power source is connected to the cathode of the end Schottky diode of the plurality of serially connected diodes, such that a precise and different voltage selection is available at each Schottky diode of the series. One of the precise voltages at the anode of one of the Schottky diodes is then connected to a circuit element to be tested as its core or operating voltage and an OBIRCH circuit analysis is then run on the circuit element to be tested in the normal manner.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0014] FIG. 1 is a prior art OBIRCH analysis setup using a first power supply to drive the OBIRCH circuitry and a second power supply to operate the circuit elements of the IC being tested;

[0015] FIG. 2 is an OBIRCH setup according to the present invention for decreasing the effects of power supply background noise and instability by using a single constant voltage power supply and a Schottky diode circuit to power both the OBIRCH analysis circuit and the circuit element under test; and

[0016] FIG. 3 is an enlarged view of the Schottky diode circuit of the present invention showing various voltages available for driving the IC elements under test.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0017] Referring now to FIG. 1, there is shown a block diagram of the prior art apparatus for carrying out an OBIRCH method of analysis. As shown, an IC (integrated circuit) 10 is supported in a package 12 having a plurality of input/output contacts such as contact 14. In the embodiment illustrated, there is also included a test fixture 16 for ease of supporting and connecting the packaged IC chip 10 during testing.

[0018] A laser 18 together with a scanning microscope 20 is used to focus a laser beam onto elements of the chip 10 as it scans an area of the chip. The scanned area is determined by a signal on control line 22 provided by controller 24. Controller 24 also includes conversion circuitry to receive a signal indicating the precise position of the laser beam as its scans the chip 10. A constant voltage power supply 26 provides a current through the wires or conductors on chip 10 being measured, and a current sensing device 28 determines, measures and amplifies the current traveling through the selected wires and conductors on chip 10. Current sensing device 28 also sends a signal indication of the sensed current to controller 24.

[0019] Also according to the prior art, there is another power supply 30 such as a model 4155 from the Hewlett Packard Company for providing selected "core" or "operating" voltages to the active current elements on chip 10. The controller 24 then provides imaging information corresponding to the sensed current at each scanning position to the display 32. The provided information is typically luminescence information corresponding to the sensed current so that an image output of the chip provides an image indication of current flow through the wires and conductors at the various scan positions.

[0020] Although suitable for some testing, the prior art arrangement of FIG. 1 is not always satisfactory when testing portions of an IC with operating active elements such as transistors and the like. This unsatisfactory operation is typically due to background noise, drift and other forms of instability of the power supply 30 with respect to the constant voltage supply 26. This noise and instability swamps the current charges due to defects in the chip so as to make the current images unreliable.

[0021] Referring now to FIG. 2, there is illustrated a new method of setting up an OBIRCH circuit analysis that overcomes these problems. Those portions of the circuit arrangement that operate similar to the prior art arrangement carry the same reference numbers used in FIG. 1. Therefore, as shown, and according to the present invention, the separate power supply 30 has been eliminated with the constant voltage power supply 26 in addition to being used as the current source for providing current through the wires and conductors of the chip 10 being tested, is now connected to a diode circuit 34, comprised of a pair of common or bipolar diodes 36 and 38 connected to a series of Schottky diodes 40-52. In the embodiment shown, each of the Schottky diodes 40-52, connected cathode-to-anode, are selected to provide a precise voltage drop so that along with the two bipolar diodes 36 and 38, the constant voltage from power supply 26 results in a series of variable voltages 56 at the anode of each of the Schottky diodes.

[0022] As an example, the voltage output from constant voltage power supply 26 used to provide a constant current is typically about 3.6 volts, and seven Schottky diodes are all precisely selected to have a forward voltage drop of 0.3 volts each. These voltages, when combined with the forward voltage drop of the two common or bipolar diodes, provide a series of stable voltages available for use as the core or operating voltage of circuit elements on IC chip 10.

Also as shown, output 56 and 58 provide additional voltage taps if needed. FIG. 3 is a more detailed illustration of the diode circuit 34.

[0023] Thus, by using constant voltage power supply 26, any background noise of the power supply 28 will be seen simultaneously at both the current source to the wires and conductors and to the core operating voltage provided to the individual elements on chip 10 so as to effectively cancel each other and provide a less distorted current image at display 32.

[0024] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that dimensions and layer thickness may be varied while remaining within the scope of the present invention.

[0025] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, methods, or steps.